

DM74LS298

Quad 2-Port Register Multiplexer with Storage

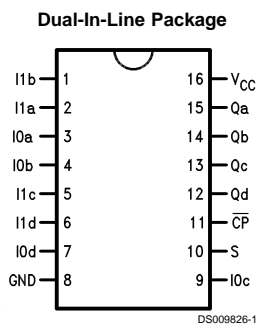
General Description

The 'LS298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

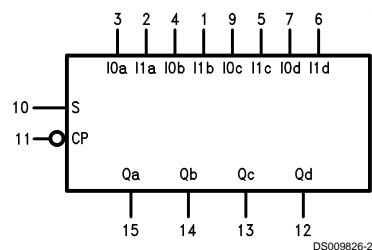
Features

- Select from two data sources
- Fully edge-triggered operation
- Typical power dissipation of 65 mW

Connection Diagram



Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Order Number DM54LS298J, DM54LS298W,
DM74LS298M or DM74LS298N
See Package Number J16A, N16E or W16A

Pin Names	Description
S	Common Select Inputs
\overline{CP}	Clock Pulse Input (Active Falling Edge)
I _{0a} , I _{0d}	Source 0 Data Inputs
I _{1a} , I _{1d}	Source 1 Data Inputs
Q _a , Q _d	Flip-Flop Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage

7V

Input Voltage

7V

Operating Free Air Temperature Range

DM54LS

DM74LS

Storage Temperature Range

–55°C to +125°C

0°C to +70°C

–65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS298			DM74LS298			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			–0.4			–0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	–55		125	0		70	°C
t_s (H)	Setup Time HIGH or LOW	25			25			ns
t_s (L)	S to \overline{CP}	25			25			
t_h (H)	Hold Time HIGH or LOW	0			0			ns
t_h (L)	S to \overline{CP}	0			0			
t_s (H)	Setup Time HIGH or LOW	15			15			ns
t_s (L)	I_{0x} or I_{1x} to \overline{CP}	15			15			
t_h (H)	Hold Time HIGH or LOW	5.0			5.0			ns
t_h (L)	I_{0x} or I_{1x} to \overline{CP}	5.0			5.0			
t_w (H)	\overline{CP} Pulse Width HIGH or LOW	20			20			ns
t_w (L)		20			20			

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			–1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}, V_{IL} = \text{Max}$	DM54 2.5			V
			DM74 2.7	3.4		
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}, V_{IH} = \text{Min}$	DM54		0.4	V
			DM74	0.35	0.5	
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$	DM74	0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 7 \text{ V}$	DM74		0.1	mA
		$V_I = 10 \text{ V}$	DM54			
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7 \text{ V}$			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			–0.4	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$	DM54	–20	–100	mA
		(Note 3)	DM74	–20	–100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}, I_{0n}, I_{1n}, S = \text{GND}, \overline{CP} = \sim$			21	mA

Note 2: All typicals are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = +5V$ and $T_A = +25^\circ C$

Symbol	Parameter	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output \overline{CP} to Q_n		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output \overline{CP} to Q_n		25	ns

Functional Description

This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

Truth Table

Inputs			Output
S	$I0_x$	$I1_x$	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

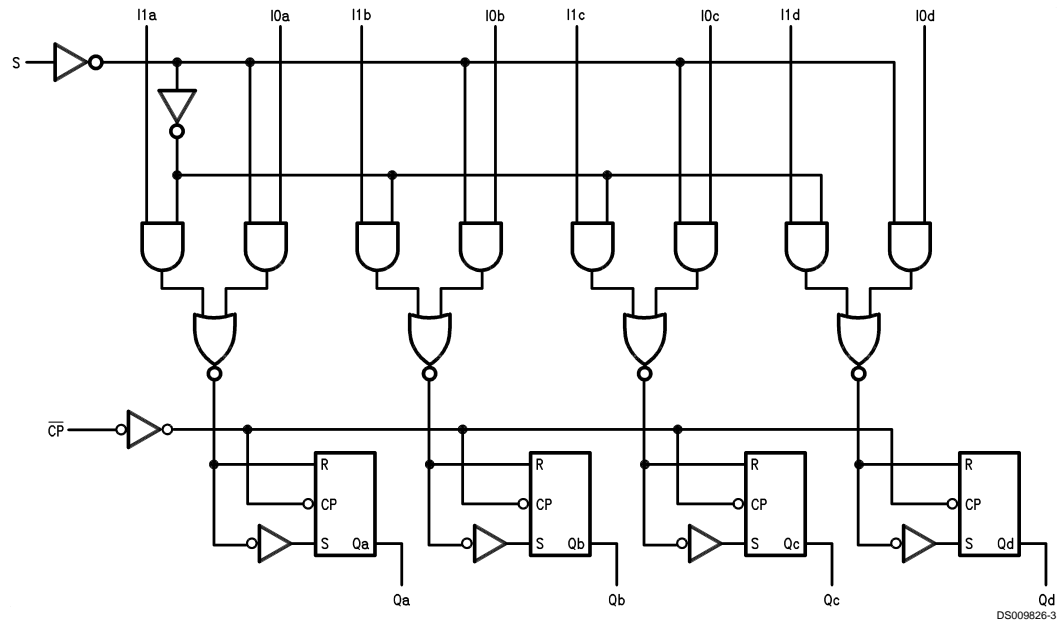
h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

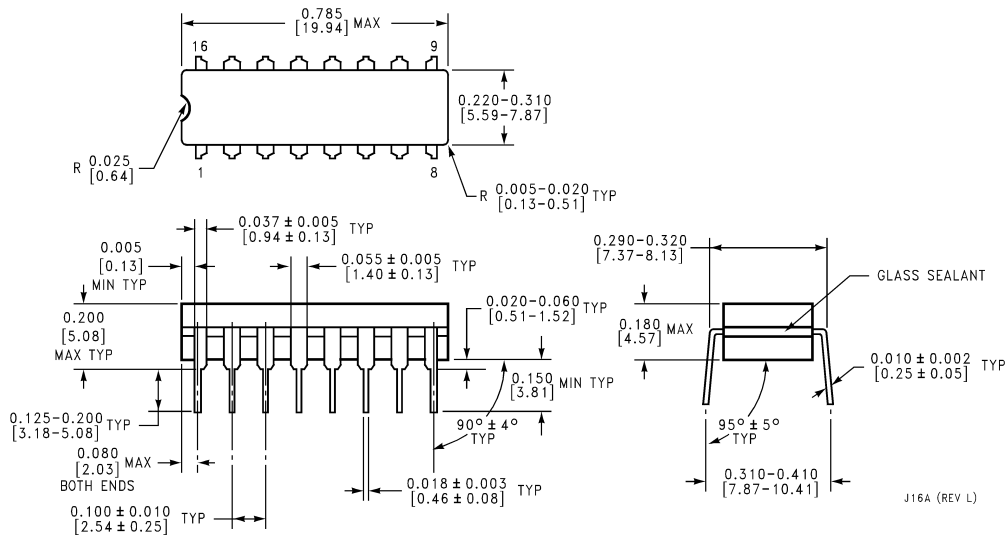
X = Immaterial

Logic Diagram

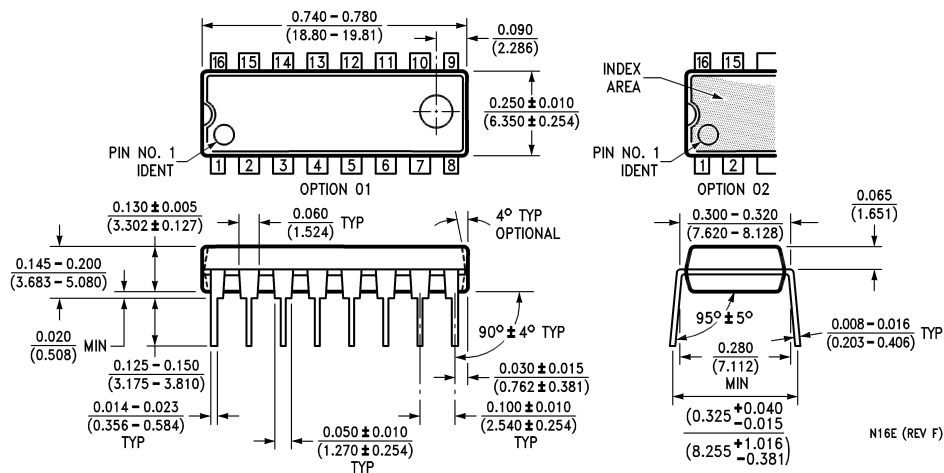




Physical Dimensions inches (millimeters) unless otherwise noted

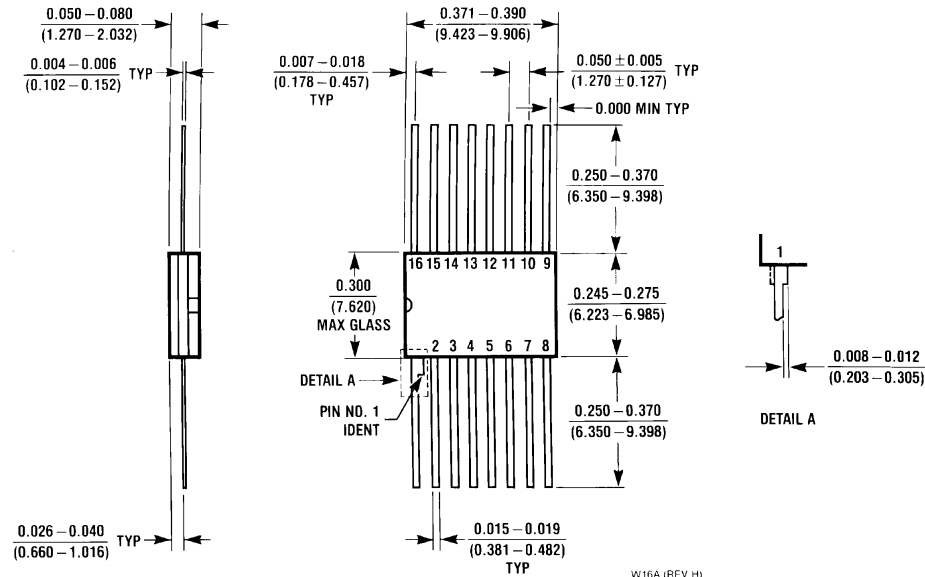


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS298J
Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS298N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54LS298W
NS Package Number W16A

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