FAIRCHILD
SEMICONDUCTOR®

SPT8100

16-BIT, 5 MSPS CMOS A/D CONVERTER

TECHNICAL DATA

JANUARY 9, 2002

FEATURES

- 16-bit, 5 MSPS CMOS analog-to-digital converter
- On-chip PGA: gain range from 0 to 19.5 dB in seven selectable settings:
  0 dB, +2.9 dB, +5.8 dB, +11.8 dB, +14.8 dB, +17.5 dB, +19.5 dB
- DLE: ±0.5 LSB, ILE: ±1.25 LSB
- SFDR: 94 dB @ f_{IN} = 900 kHz, –8.1 dBFS
- Internal sample-and-hold and voltage reference
- Power dissipation: 465 mW at 5 MSPS
- +5 V analog supply and +3.3 to +5.25 V digital output supply
- 44-lead LQFP plastic package

APPLICATIONS

- Data acquisition systems
- IR imaging
- Scanners and digital copiers
- High-end CCD cameras
- Medical imaging
- Wireless communications
- Lab and test equipment
- Automatic test equipment

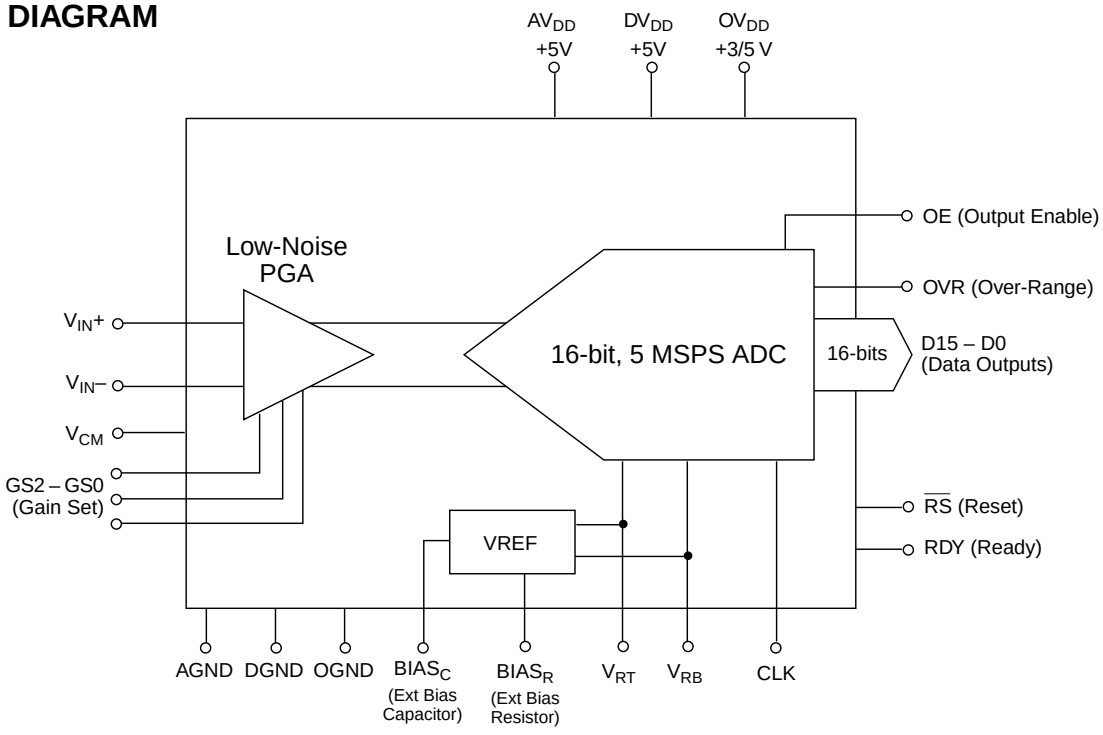
DESCRIPTION

The SPT8100 is a high-performance, 16-bit analog-to-digital converter that operates at a sample rate of up to 5 MSPS. Excellent dynamic performance and high linearity is achieved by a digitally calibrated pipelined architecture fabricated in CMOS process technology.

A low-noise programmable gain amplifier (PGA) is also incorporated on chip. The PGA is digitally programmable in seven selected settings over a 0 to +19.5 dB range. The SPT8100 also features an on-chip internal sample-and-hold and internal reference for minimal external circuitry.

It operates from a single +5 V supply. Total power dissipation, including internal reference, is 465 mW. A separate digital output supply pin is provided for +3.3 V or 5 V logic output levels. The SPT8100 is available in a 44-lead LQFP package over the industrial temperature range of –40 °C to +85 °C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V
OV_{DD} ..... +6 V

Input Voltages

Analog Input ..... –0.5 V to V_{DD} +0.5 V
CLK Input ..... V_{DD}
$AV_{DD} – DV_{DD}$ ..... ±100 mV
Delta between AGND, DGND, and OGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... –40 to +85 °C
Junction Temperature ..... +175 °C
Lead Temperature (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD}=DV_{DD}$=+5.0 V, OV_{DD}= 3.3 V, f_S=5 MSPS, 2.5 V_{PP} input span, Gain=0 dB, R_{EXT}=1.43 kΩ, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT8100 MIN	SPT8100 TYP	SPT8100 MAX	UNITS
Resolution			15.9	16		Bits
DC Accuracy						
Integral Linearity Error (ILE)		V		±1.25		LSB
Differential Linearity Error (DLE)		V		±0.5		LSB
Gain Error[1]		IV	–7.5		+7.5	%FSR
Offset Error[2]		IV	–5		+5	%FSR
Analog Input (into PGA)						
Differential Input Voltage Range						
$V_{IN}+$, $V_{IN}–$		V		5		V_{PPD}
Input Capacitance		IV			15	pF
Input Resistance[3]	PGA Gain = 0 dB	IV		5.5		kΩ
Input Bandwidth[4]	PGA Gain = 0 dB	V		12		MHz
Input Common Mode Voltage Range		V	1.15	2.40	3.65	V
Programmable Gain Amp						
Composite Input-Referred	f_{IN} > 300 kHz					
Noise Floor	PGA Gain = 0 dB	V		1.4		LSB_{RMS}
	PGA Gain = 2.9 dB	V		1.5		LSB_{RMS}
	PGA Gain = 5.8 dB	V		1.6		LSB_{RMS}
	PGA Gain = 11.8 dB	V		2.0		LSB_{RMS}
	PGA Gain = 14.8 dB	V		2.3		LSB_{RMS}
	PGA Gain = 17.5 dB	V		2.6		LSB_{RMS}
	PGA Gain = 19.5 dB	V		2.8		LSB_{RMS}
PGA Range		V		19.5		dB
PGA Gain Steps[3]		VI		0,2.9,5.8,11.8,14.8,17.5,19.5		dB
PGA Gain Accuracy		VI		±0.3		dB
Conversion Characteristics						
Maximum Conversion Rate		VI	5			MSPS
Pipeline Delay (Latency)[5]		IV			5.5	Clocks
Reset Pulse Time ($\overline{RS}$)		IV	3			Clocks
Reset Calibration Time	FS = 5 MSPS	V		150		ms
References and External Bias						
$V_{RT} – V_{RB}$ (Internal Ref)		VI	2.375	2.5	2.625	V
Bias Resistor Range (External)		V	800	1430	2500	Ω
V_{CM} Output Voltage		IV	2.275	2.40	2.525	V
V_{CM} Output Current		IV			47	µA
V_{RT}		V	3.45	3.65	3.85	V
V_{RB}		V	0.95	1.15	1.35	V

[1] Total gain error of PGA and ADC using internal references.
[2] Total offset error of PGA and ADC relative to mid-scale.
[3] See table I for input resistance as a function of PGA gain.
[4] Input bandwidth is a frequency to which the fundamental energy drops by 3 dB
[5] The input is sampled on the falling edge of the clock and is available on the output after the rising edge of the clock, 5.5 clock cycles later.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, AV_{DD}=DV_{DD}=+5.0 V, OV_{DD}= 3.3 V, f_S=5 MSPS, 2.5 V_{PP} input span, Gain=0 dB, R_{EXT}=1.43 kΩ, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT8100 MIN	SPT8100 TYP	SPT8100 MAX	UNITS
Dynamic Performance[1]						
Effective Number of Bits	ADC Input = –1 dBFS[2]					
f_{IN} = 60 kHz		IV	12.2	13.0		Bits
f_{IN} = 900 kHz		V		12.7		Bits
Signal-to-Noise Ratio (without Harmonics)	ADC Input = –1 dBFS[2]					
f_{IN} = 75 kHz		IV	78	81		dB
f_{IN} = 900 kHz		V		80		dB
Harmonic Distortion	ADC Input = –0.5 dBFS					
f_{IN} = 60 kHz		IV		–92	–84	dB
f_{IN} = 900 kHz		V		–82		dB
Signal-to-Noise and Distortion (SINAD)	ADC Input = –1 dBFS					
f_{IN} = 60 kHz		IV	75	80		dB
f_{IN} = 900 kHz		V		78		dB
Spurious Free Dynamic Range[3]						
f_{IN} = 60 kHz	ADC Input = –0.5 dB	IV	85	94		dBc
f_{IN} = 900 kHz		V		94		dBc
f_{IN} = 2 MHz	R_{EXT} = 1 kΩ @ 10 MSPS	V		83		dBc
f_{IN} = 3 MHz	R_{EXT} = 1 kΩ @ 10 MSPS	V		78		dBc
Two-Tone Intermodulation						
3rd Order Distortion	f_1=400 kHz, f_2=410 kHz[4]	V		–94		dB
	f_1=890 kHz, f_2=900 kHz[5]	V		–89		dB
Inputs						
GS0–GS2 Logic 1 Voltage		VI	2.4			V
GS0–GS2 Logic 0 Voltage		VI			0.8	V
CLK, $\overline{RS}$ Logic 1 Voltage		VI	2.0			V
CLK, $\overline{RS}$ Logic 0 Voltage		VI			0.8	V
Maximum Input Current Low		VI	–10		+10	µA
Maximum Input Current High		VI	–10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic 1 Voltage	I_{OH} = –2 mA	VI	OV_{DD} – 0.5			V
Logic 0 Voltage	I_{OL} = 2 mA	VI			0.4	V
CLK to Output Delay Time (t_D)	C_{LOAD} = 20 pF	IV			30	ns
Power Supply Requirements						
Voltages OV_{DD}		IV	3.0	3.3	5.25	V
AV_{DD}		IV	4.75	5.0	5.25	V
DV_{DD}		IV	4.75	5.0	5.25	V
Currents I_{DD}		VI		93	103	mA
Power Dissipation		VI		465	515	mW

[1] Dynamic performance tested at f_S=4.4 MSPS

[2] 0 dBFS is 5.0 V peak-to-peak differential

[3] ADC Input = –8.1 dBFS, unless otherwise noted

[4] Test Conditions: PGA setting of 5.8 dB; Analog Input at ADC = –0.7 dB

[5] Test Conditions: PGA setting of 0 dB; Analog Input at ADC = –1.9 dB

TEST LEVEL CODES	TEST LEVEL	TEST PROCEDURE
All electrical characteristics are subject to the following conditions:	I	100% production tested at the specified temperature.
	II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.	III	QA sample tested only at the specified temperatures.
	IV	Parameter is guaranteed (but not tested) by design and characterization data.
	V	Parameter is a typical value for information purposes only.
	VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

DEVICE OVERVIEW

The SPT8100 combines a high-resolution 5 MSPS 16-bit ADC, a built-in reference, and a programmable gain amplifier (PGA) with resistive input impedance in a 44-pin package.

The device includes a digitally calibrated pipeline ADC, which is calibrated on assertion of a simple reset signal. The combination of low noise, high linearity, a high-input impedance buffer (with programmable gain), wideband S/H, on-board voltage references, and simple digital interface (16-bit parallel output word synchronous with the master sampling clock) makes the SPT8100 extremely easy to use in a wide variety of systems.

For optimum performance, the analog inputs should be driven differentially, and may be AC-coupled or DC-coupled to a source. Typical applications include high-performance data acquisition systems, automatic test equipment, and wideband digital communications receivers such as wireless basestations.

OPERATIONAL DESCRIPTION

The following sections describe in greater detail individual blocks and functions of the SPT8100.

The incoming analog differential signal (maximum level 5 V peak-to-peak differential) enters the device at the pins $V_{IN}+/V_{IN}-$. The analog signal path is partitioned into a programmable gain amplifier (PGA) and an ADC. The PGA has maximum gain of +19.5 dB; the gain is set by the digital control signals GS0 to GS2.

The output of the PGA is fed directly to the ADC, which samples at a rate equal to the CLK frequency and outputs a 16-bit wide parallel word. The ADC uses a pipeline multistage architecture. Latency is 5.5 clock cycles.

ADC CLOCK

The chip requires a single low-jitter clock to be applied at the CLK pin, with nominal 40–60% duty cycle. All clock generation is performed internally and all converter and S/H clocks in the ADC path are directly derived from CLK.

If the sample rate is changed by more than a factor of 2, the device must be recalibrated using the $\overline{RS}$ (reset) pin.

DEVICE STARTUP/INITIALIZATION SEQUENCE

Note: This initialization sequence is *required*. Without it, the device will not work.

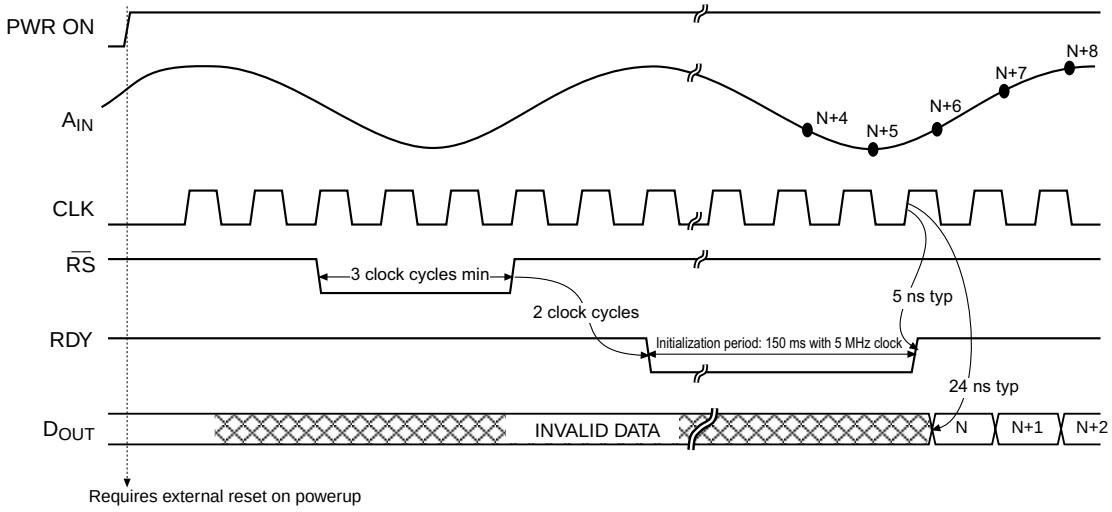
Allow sufficient time for the analog blocks on the SPT8100 to power on and come up to their quiescent DC states. Allowance may also be needed for thermal time constants associated with the package/board.

On powerup, the SPT8100's $\overline{RS}$ (reset) should be held low for at least three clock cycles. The power supply voltages applied to the device must be stable during this time. The clock signal (CLK) must be running for at least three clock cycles prior to the rising edge of $\overline{RS}$, and must continue running.

When the $\overline{RS}$ signal goes from low to high, calibration is initiated. RDY is driven low two clock cycles after the rising edge of $\overline{RS}$, and will stay low for 150 ms with a 5 MHz clock. When the initialization is complete, RDY returns high and the device is ready for normal operation. Note that the calibration of the ADC can be interrupted (before completion) by changing the $\overline{RS}$ signal from high to low, which will cause another reset to occur. When $\overline{RS}$ goes from low back to high, another calibration cycle will begin.

RDY cannot be tri-stated: it is always driven either high or low. The CLK must be constantly running throughout the

Figure 1 – Device Initialization Timing



initialization phase until RDY is deasserted. Note that, although typically the device is initialized when power is first applied, the initialization is only started when the $\overline{RS}$ is asserted; there is no "power-on-reset" circuitry on chip. $\overline{RS}$ may be held low for an indefinite period of time. While $\overline{RS}$ is low, RDY will remain high. After $\overline{RS}$ is returned to high, RDY will go low for the duration of the calibration.

PROGRAMMABLE GAIN AMPLIFIER

The programmable gain amplifier (PGA) precedes the ADC inputs. The differential inputs, which are resistive, are at pins V_{IN}+ and V_{IN}–. The maximum input range is 5 V peak-to-peak differential (2.5 V single-ended). To achieve maximum overall system noise performance, the source driving these inputs needs to be as low-noise and as low-jitter as possible, while maintaining the required distortion performance. In addition, the driving source must be low impedance to maintain the accuracy of the PGA gain.

The internal 0 dB analog signal level and ADC full-scale output level is 5 V peak-to-peak differential (2.5 V single-ended). The PGA may be used to provide gain for an input less than 5 V peak-to-peak differential.

The gain of the PGA can be programmed using a three-bit control, available at pins GS0 to GS2. See table I. Note that the input resistance is a function of the gain setting.

Table I – PGA Gain Control

GS2	GS1	GS0	PGA Gain (dB)	Input Resistance (kΩ)	V/V Gain	3 dB BW	LSB_{RMS}
0	0	0	0	5.57	1	12	1.4
0	0	1	2.9	4.65	1.40	10	1.5
0	1	0	5.8	3.97	1.95	8	1.6
0	1	1	11.8	2.23	3.9	7	2.0
1	0	0	14.8	1.66	5.5	6	2.3
1	0	1	17.5	1.25	7.5	5.5	2.6
1	1	0	19.5	1.00	9.5	5	2.8
1	1	1	X	Forbidden			

TYPICAL INTERFACE CIRCUIT

ANALOG INPUT DRIVER

The differential analog inputs (V_{IN}+, V_{IN}–) have a resistive input impedance of 1 kΩ minimum. For best performance, the input source should be a differential input, as shown in figure 2, typical interface circuit. The SPT8100 provides its own common-mode voltage on the pin marked V_{CM}. Output drive capability of V_{CM} is a maximum of 47 µA (50 kΩ to ground).

The SPT8100 application note (AN8100) shows an example of two modes of driving the SPT8100. One mode is through a transformer and the other is through a single-to-differential converter. In all cases, both inputs V_{IN}+ and V_{IN}– must be kept within the input common-mode range (1.15 V to 3.65 V).

$BIAS_C$ CONNECTION

An external capacitor, C_{EXT} on the $BIAS_C$ pin, is used only for noise filtering of an internal voltage associated with the references. Its value is not critical: 1 µF in parallel with 0.01 µF is recommended.

$BIAS_R$ CONNECTION

As shown in the typical interface circuit, R_{EXT} is needed to connect between $BIAS_R$ to ground. This resistor ranges from 800 Ω to 2.5 kΩ. The proper selection of R_{EXT} is a function of the sample rate and input frequency. Nominally, at 5 MSPS, R_{EXT}=1.43 kΩ is recommended. If linearity for large signal levels at an analog bandwidth of 2 MHz is critical, the value should be decreased to R_{EXT}=1.24 kΩ; and for even higher-frequency analog inputs, R_{EXT}=1.0 kΩ can be used. At lower sample rates (for example 2 MSPS), and lower analog input frequencies, the value may be increased to R_{EXT}=2 kΩ. (Refer to the typical interface circuit table in figure 2b.)

POWER SUPPLIES AND GROUNDING

The SPT8100 requires three power supplies: analog AV_{DD}, digital DV_{DD} and output supply OV_{DD}. This device works best if all three supplies are coming from the analog supply side of the system as shown in the typical interface circuit (figure 2a).

Note, in figure 2a, that the supplies to the logic interface circuit and the OV_{DD} are separate from each other. In a case where the +A3.3/5 V supply is not available, try to implement the design as close as possible to that shown in figure 2b. Place the ferrite bead (FB1) as close to the device as possible. To avoid latch-up, the delta between all three grounds must stay with 100 mV; this includes transients. (Refer to the absolute maximum ratings specifications.)

Figure 2a – Typical Interface Circuit

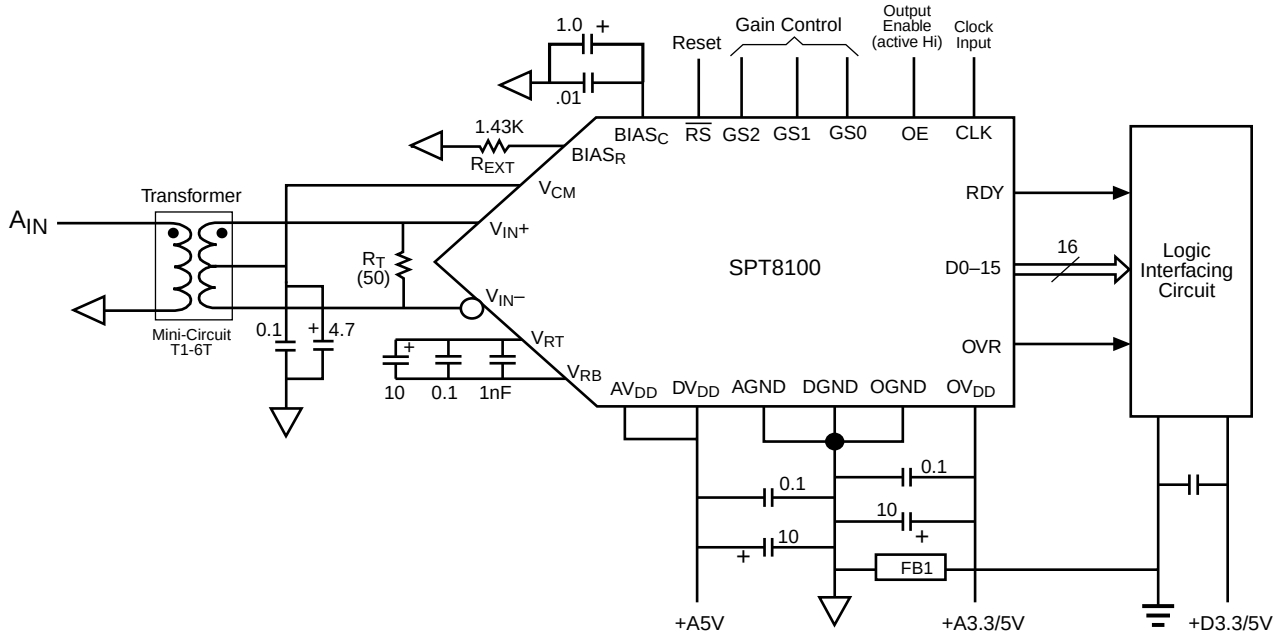
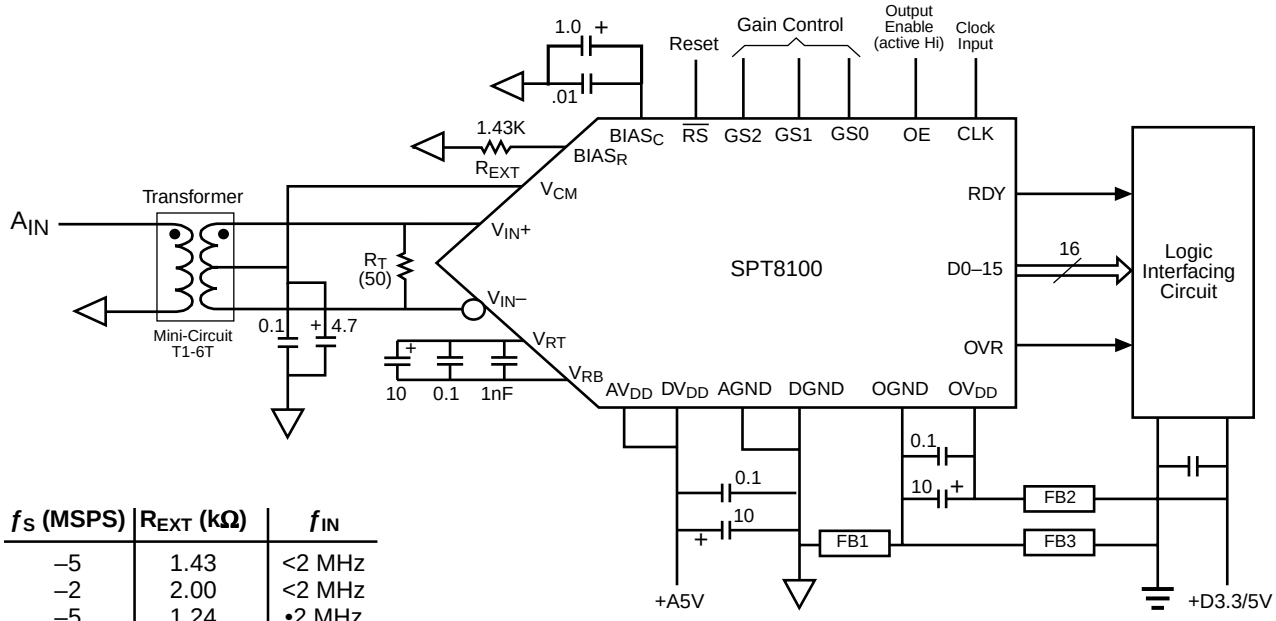


Figure 2b – Typical Interface Circuit



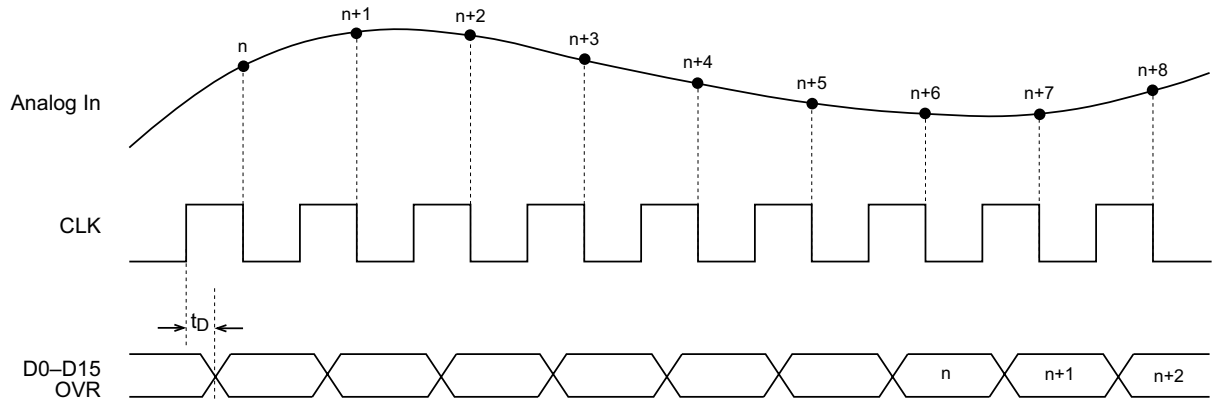
f_S (MSPS)	R_{EXT} (kΩ)	f_{IN}
–5	1.43	<2 MHz
–2	2.00	<2 MHz
–5	1.24	•2 MHz
–2	1.00	•2 MHz

800 Ω – R_{EXT} – 2.5 kΩ

Notes:

1. To avoid device latch-up, closely follow either figure 2a or 2b, depending on what is available in the system. The difference between figure 2a and 2b is in the grounding.
2. FB = ferrite bead. FB1 must be placed as close to the device as possible.
3. R_{EXT} = 1.43 kΩ, optimized for f_S = 5 MSPS. Refer to the above table for recommended value of R_{EXT} with respect to f_S and f_{IN}.
4. R_T is A_{IN} source termination resistor.
5. Power supplies and references pins must have adequate decoupling. Surface-mount capacitors are highly recommended. The smallest value of capacitors are to be placed as close to the pin as possible.

Figure 3 – Timing Diagram 1



INPUT/OUTPUT TIMING

The SPT8100 implements a simple interface: the 16 ADC outputs appear on the pins D15–D0 as a parallel word synchronous with the ADC sampling clock. D0 is the LSB and D15 is the MSB. The timing diagram for the ADC digital outputs is shown in figure 3. The data is sampled at the falling edge of the clock. The ADC sampling clock is at the same frequency as CLK.

The output data is updated on the rising edge of CLK with a clock latency of 5.5 clock cycles.

OUTPUT LOGIC LEVEL

The voltage levels on the D15–D0 lines and OVR are CMOS levels: the HIGH level is determined by the power supply voltage on the OV_{DD} pin, which can be set independently of the other supply pins on the device over the range from 3.0 V to 5.25 V (3.3 V typical). The RDY pin level is determined by DV_{DD} (+5 V).The external digital output buffers should be placed as close as possible to the SPT8100 digital outputs to minimize any line reflections that would cause performance degradation.

ADC REFERENCES

The ADC full-scale range is set by reference voltages generated on chip. These two reference voltages appear on pins V_{RT} and V_{RB}; nominally their difference is 2.5 V. The references are not designed to be overdriven. The V_{RT} and V_{RB} pins should be very carefully decoupled on the board using as short a trace as possible. Some optimization of the decoupling may be required, as shown in the typical interface circuit diagram. The smallest capacitor should be the closest one to the chip. (Refer to the typical interface circuit diagram.)

OUTPUT ENABLE

The ADC digital outputs are enabled by the active high output enable pin (OE).

OE = 1: ADC digital outputs are enabled

OE = 0: ADC digital outputs are high-impedance (tri-stated)

DIGITAL CODE RANGE AND OUT-OF-RANGE DETECTION

The output format of the ADC digital data is offset binary. Due to the calibration algorithm used, there is a slight loss in digital code range from the ADC. Instead of FFFFH and 0000H at the extremes of the range, the actual maximum and minimum codes are less than that by 1.6% at both ends of the scale, and vary from chip to chip. Effectively, this is a loss in dynamic range of a few tenths of a dB, and is negligible in many applications. The out-of-range function is defined accordingly, and sets the state of the active high digital output OVR, as follows:

OVR is HIGH if the ADC digital code is greater than or equal to FC00H or less than or equal to 03FFH. (See figure 4.)

If the output code exceeds FC00(max) or 03FF(min), this implies that output is clipping. Therefore, once these limits are crossed, the second harmonic becomes significant and degrades performance.

Figure 4 – ADC Digital Code Range and Overrange Bit Function

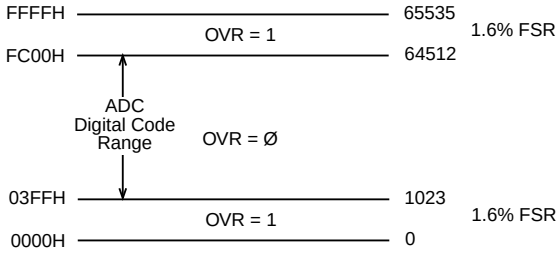


Figure 5 – Timing Diagram 2

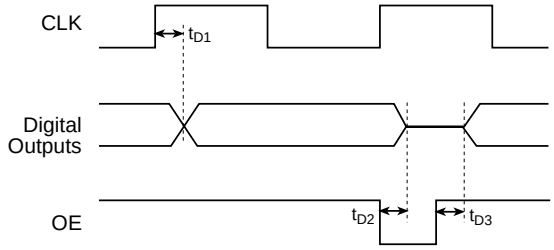
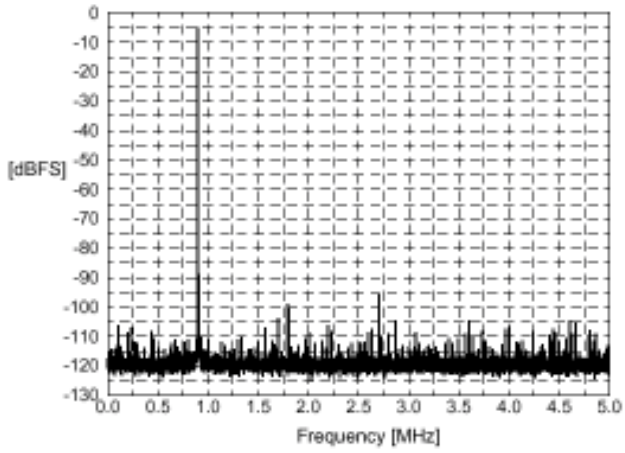


Table II – Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
CLK high to Data Valid	t_{D1}	18	24	40[1]	ns
OE inactive to HiZ	t_{D2}	10	16	30	ns
OE active to Data Valid	t_{D3}	10	16	30	ns

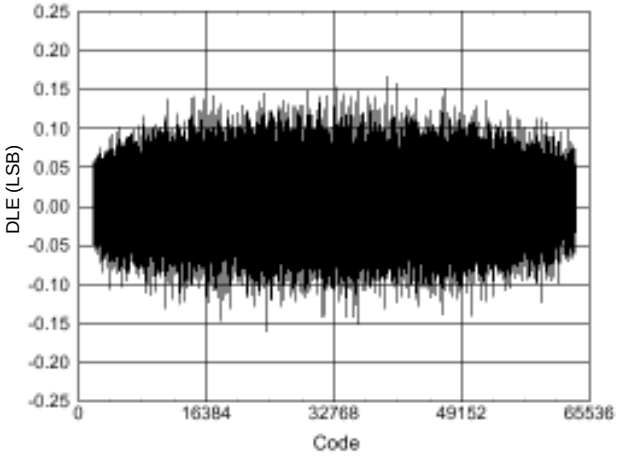
[1] Conditions: load capacitance = 20 pF, V_{OH} = 3.3 V

FFT Plot



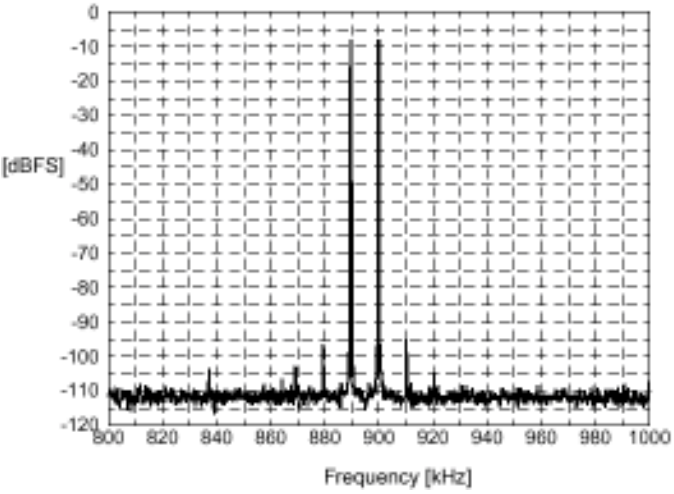
Test Conditions:
f_{IN} = 2 MHz
f_{CLK} = 4.4 MHz
PGA Gain = 18 dB
R_{EXT} = 1.08 kΩ
ADC Input (Post PGA) = –5.4 dBFS
T_A = +25 °C

Typical Differential Linearity Error (DLE)



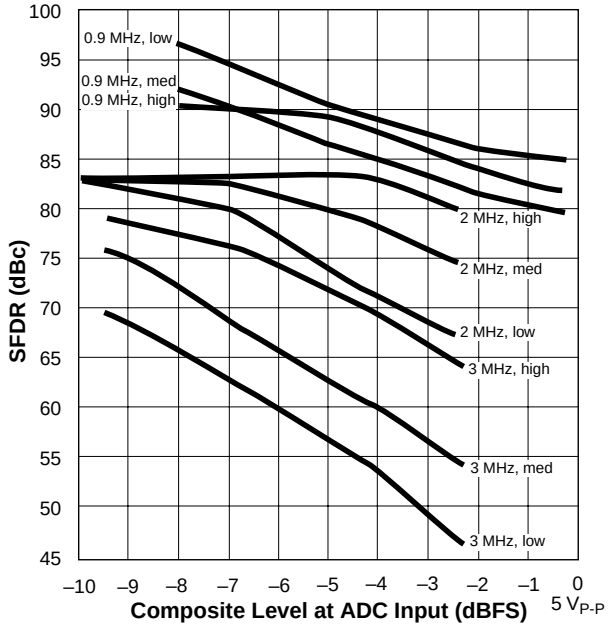
Test Conditions:
f_{IN} = 75 kHz
f_{CLK} = 4.4 MHz
PGA Gain = 0 dB
Near Full-Scale Input

Two-Tone Intermodulation FFT



Test Conditions:
f_1 = 890 kHz
f_2 = 900 kHz
f_{CLK} = 4.4 MHz
PGA Gain = 6 dB
R_{EXT} = 1.43 kΩ
ADC Input (Post PGA) = –8.0 dBFS
T_A = +25 °C

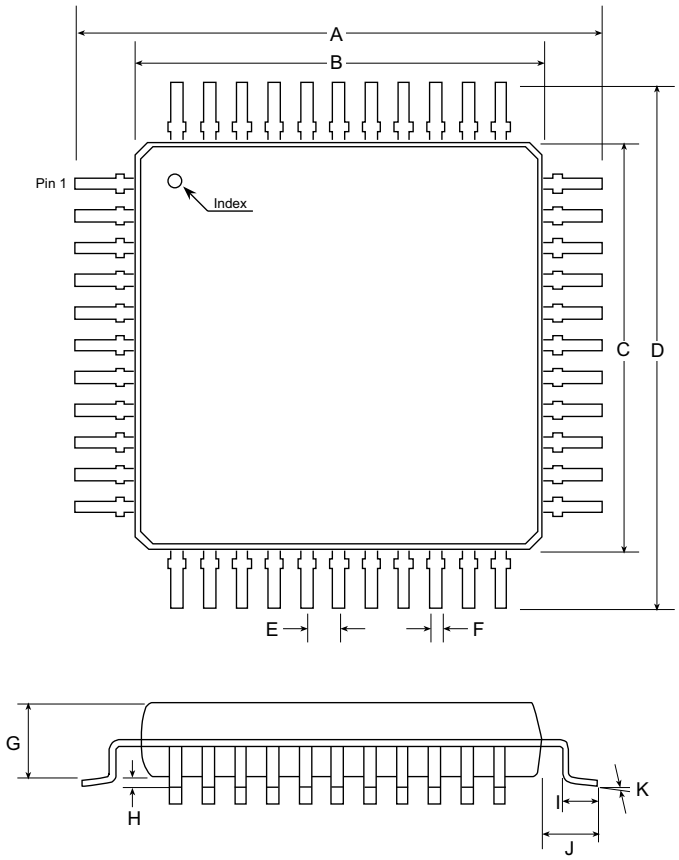
Spurious-Free Dynamic Range



Test Conditions:
10 MSPS, 5 V, 25 °C
Low: R_{EXT}=1.43 kΩ @96 mA
Med: R_{EXT}=1.24 kΩ @109 mA
High: R_{EXT}=1 kΩ @129 mA

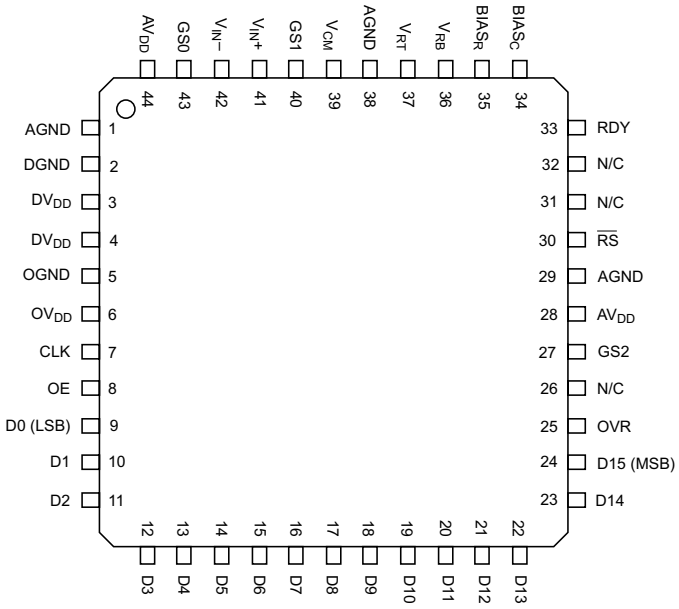
PACKAGE OUTLINE

44-Lead LQFP



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.465	0.480	11.80	12.20
B	0.390	0.398	9.90	10.10
C	0.390	0.398	9.90	10.10
D	0.465	0.480	11.80	12.20
E	0.0315 BSC		0.80 BSC	
F	0.012	0.018	0.30	0.45
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.018	0.030	0.45	0.75
J	0.039 typ		1.0 typ	
K	0–7°		0–7°	

PIN ASSIGNMENTS



PIN FUNCTIONS

Pin Name	Description
AGND	Analog ground
DGND	Digital ground
DV_{DD}	Digital +5.0 V supply
OGND	Ground for digital I/O
OV_{DD}	Digital outputs supply (+3.3/5 V)
CLK	Master reference clock
OE	Output enable (active high)
D0–D15	Data output bits; D0 is LSB; D15 is MSB
OVR	Overrange indicator bit (active high)
N/C	No connect
GS[2:0]	3-bit PGA gain setting control inputs
AV_{DD}	Analog +5.0 V supply
$\overline{RS}$	Resets internal state of chip (active low)
RDY	Initialization in progress indicator; RDY goes low during reset initialization. Chip is ready for normal operation when RDY is high.
$BIAS_C$	External bias capacitor connection
$BIAS_R$	External bias resistor connection
V_{RT}, V_{RB}	ADC reference voltage outputs
V_{CM}	Common mode reference voltage output
$V_{IN}+, V_{IN}–$	Analog inputs to the PGA

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT8100SIT	–40 to +85 °C	44L LQFP

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