MOTOROLA
**SEMICONDUCTOR**
TECHNICAL DATA

# Power Field Effect Transistor
## N-Channel Enhancement-Mode Silicon Gate TMOS

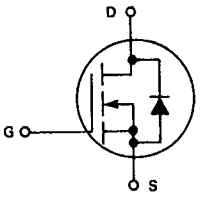
**IRF820**
**IRF821**
**IRF823**

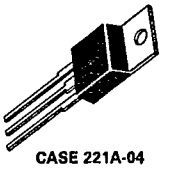
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

**TMOS POWER FETs**
**2 and 2.5 AMPERES**
**$r_{DS(on)}$ = 3 OHM**
**450 and 500 VOLTS**
**$r_{DS(on)}$ = 4 OHM**
**450 VOLTS**



**CASE 221A-04**
**TO-220AB**

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### MAXIMUM RATINGS

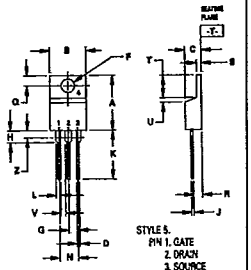
| Rating | Symbol | IRF 820 | IRF 821 | IRF 823 | Unit |
|---|---|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 500 | 450 | 450 | Vdc |
| Drain-Gate Voltage ($R_{GS}$ = 1 MΩ) | $V_{DGR}$ | 500 | 450 | 450 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | ±20 | | | Vdc |
| Drain Current Continuous Pulsed | $I_D$ $I_{DM}$ | 2.5 10 | | 2 8 | Adc |
| Total Power Dissipation @ $T_C$ = 25°C Derate above 25°C | $P_D$ | 40 0.32 | | | Adc |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to 150 | | | °C |

### THERMAL CHARACTERISTICS

| | | | |
|---|---|---|---|
| Thermal Resistance Junction to Case Junction to Ambient | $R_{\theta JC}$ $R_{\theta JA}$ | 3.12 62.5 | °C/W |
| Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds | $T_L$ | 300 | °C |

See the MTP3N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

### OUTLINE DIMENSIONS




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 14.48 | 15.75 | 0.570 | 0.620 |
| B | 9.66 | 10.28 | 0.380 | 0.405 |
| C | 4.07 | 4.82 | 0.160 | 0.190 |
| D | 0.64 | 0.88 | 0.025 | 0.035 |
| F | 3.61 | 3.73 | 0.142 | 0.147 |
| G | 2.47 | 2.66 | 0.095 | 0.105 |
| H | 2.80 | 3.93 | 0.110 | 0.155 |
| J | 0.36 | 0.55 | 0.014 | 0.022 |
| K | 12.70 | 14.27 | 0.500 | 0.562 |
| L | 1.15 | 1.39 | 0.045 | 0.055 |
| N | 4.83 | 5.33 | 0.190 | 0.210 |
| Q | 2.54 | 3.04 | 0.100 | 0.120 |
| R | 2.04 | 2.79 | 0.080 | 0.110 |
| S | 1.15 | 1.39 | 0.045 | 0.055 |
| T | 5.97 | 6.47 | 0.235 | 0.255 |
| U | 0.00 | 1.27 | 0.000 | 0.050 |
| V | 1.15 | — | 0.045 | — |
| Z | — | 2.04 | — | 0.080 |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 0.25 mA) | IRF821, IRF823<br>IRF820 | $V_{(BR)DSS}$ | 450<br>500 | —<br>— | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0)<br>($V_{DS}$ = 0.8 Rated $V_{DSS}$, $V_{GS}$ = 0, $T_J$ = 125°C) | | $I_{DSS}$ | —<br>— | 0.25<br>1 | mAdc |
| Gate-Body Leakage Current, Forward ($V_{GSF}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSF}$ | — | 500 | nAdc |
| Gate-Body Leakage Current, Reverse ($V_{GSR}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSR}$ | — | 500 | nAdc |
| **ON CHARACTERISTICS*** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mA) | | $V_{GS(th)}$ | 2 | 4 | Vdc |
| Static Drain-Source On-Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 1 Adc) | IRF820, IRF821<br>IRF823 | $r_{DS(on)}$ | —<br>— | 3<br>4 | Ohm |
| On-State Drain Current ($V_{GS}$ = 10 V)<br>($V_{DS}$ ≥ 7.5 Vdc)<br>($V_{DS}$ ≥ 8 Vdc) | IRF820, IRF821<br>IRF823 | $I_{D(on)}$ | 2.5<br>2 | —<br>— | Adc |
| Forward Transconductance<br>($V_{DS}$ ≥ 7.5 V, $I_D$ = 1 A)<br>($V_{DS}$ ≥ 8 V, $I_D$ = 1 A) | IRF820, IRF821<br>IRF823 | $g_{FS}$ | 1<br>1 | —<br>— | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1 MHz) | $C_{iss}$ | — | 400 | pF |
| Output Capacitance | | $C_{oss}$ | — | 150 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | — | 40 | |
| **SWITCHING CHARACTERISTICS*** | | | | | |
| Turn-On Delay Time | ($V_{DD}$ ≈ 200 V, $I_D$ = 1 Apk, $R_{gen}$ = 50 Ohms) | $t_{d(on)}$ | — | 60 | ns |
| Rise Time | | $t_r$ | — | 50 | |
| Turn-Off Delay Time | | $t_{d(off)}$ | — | 60 | |
| Fall Time | | $t_f$ | — | 30 | |
| Total Gate Charge | ($V_{GS}$ = 10 V, $V_{DS}$ = 0.8 x Rated $V_{DSS}$, $I_D$ = Rated $I_D$) | $Q_g$ | 12 (Typ) | 15 | nC |
| Gate-Source Charge | | $Q_{gs}$ | 6 (Typ) | — | |
| Gate-Drain Charge | | $Q_{gd}$ | 6 (Typ) | — | |
| **SOURCE-DRAIN DIODE CHARACTERISTICS*** | | | | | |
| Forward On-Voltage | ($I_S$ = Rated $I_D$, $V_{GS}$ = 0) | $V_{SD}$ | — | 1.5(1) | Vdc |
| Forward Turn-On Time | | $t_{on}$ | Limited by stray inductance | | |
| Reverse Recovery Time | | $t_{rr}$ | 500 (Typ) | — | ns |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from the contact screw on tab to center of die)<br>(Measured from the drain lead 0.25" from package to center of die) | | $L_d$ | 3.5 (Typ)<br>4.5 (Typ) | —<br>— | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25" from package to source bond pad) | | $L_s$ | 7.5 (Typ) | — | |

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.1 V for IRF820 and IRF821.