CMOS IC

SANYO

LC7152, 7152M, 7152NM, 7152KM

Universal Dual-PLL Frequency Synthesizers



Overview

The LC7152, 7152M, 7152NM, 7152KM are universal dual-PLL frequency synthesizers for use in weak signal type cordless telephone applications in the USA, South Korea, and Japan, and broadcast satellite (BS) tuners in the USA and Europe.

Features

- Dual charge pump built in for fast channel switching
- Digital lock detector enables PLL lock status check with crystal oscillator precision
- Programmable reference frequency divider supports various applications
- The LC7152NM is a built-in power-on reset circuit version of the LC7152M
- The LC7152KM is an enhanced frequency characteristics version of the LC7152M

Functions

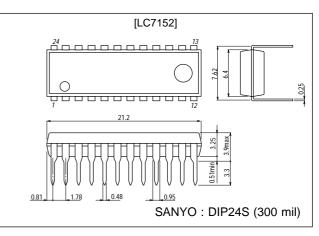
- 2-system PLL built-in (dual PLL)
- 16-bit programmable local-oscillator divider 1.5 to 55 MHz (V_{DD} = 2.0 to 3.3 V), LC7152KM: 55 to 80 MHz (V_{DD} = 2.7 to 3.3 V)
- 14-bit programmable reference-frequency divider 320 Hz to 640 kHz reference frequency using a 10.24 MHz crystal oscillator
- · Digital lock detector
- Dual charge pump
- Amplifier built-in for an active LPF
- Serial transmission data input (CCB format)
- LC7152NM with power-on reset circuit (pins OUTA and OUTB become open at power-on)
- 2.0 to 3.3 V supply voltage
- DIP24S and MFP24S packages

CCB is a trademark of SANYO ELECTRIC CO., LTD.
CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

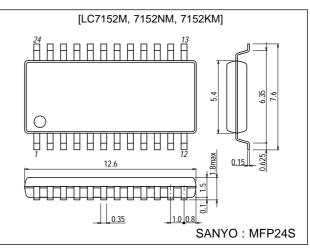
unit : mm

3067-DIP24S



unit : mm

3112-MFP24S



- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co.,Ltd. Semiconductor Company TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25° C, V_{SS} = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|------------------------|-------------------------------------|------------------------------|------|
| Maximum supply voltage | V _{DD} max | V _{DD} | -0.3 to +7.0 | V |
| Maximum input valtage | V _{IN} max(1) | CE, CL, DI, AIA, AIB | -0.3 to +7.0 | V |
| Maximum input voltage | V _{IN} max(2) | XIN, PIA, PIB, TEST | –0.3 to V _{DD} +0.3 | V |
| | V _O max(1) | LDI, LDB | -0.3 to +7.0 | V |
| Maximum output voltage | V _O max(2) | AOA, AOB, OUTA, OUTB | -0.3 to +15 | V |
| | V _O max(3) | PDA1, PDA2, PDB1, PDB2, XOUT | –0.3 to V _{DD} +0.3 | V |
| Movimum output ourroat | I _O max(1) | LDA, LDB, OUTA, OUTB | 0 to 3 | mA |
| Maximum output current | I _O max(2) | AOA, AOB | 0 to 6 | mA |
| | | Ta≦85°C, LC7152 | 350 | mW |
| Allowable power dissipation | Pd max | Ta≦85°C, LC7152M, 7152NM, 7152KM | 160 | mW |
| Operating temperature | Topr | | -40 to +85 | °C |
| Storage temperature | Tstg | | -55 to +125 | °C |

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

| Deremeter | Symbol | Conditions | | Ratings | | Unit |
|------------------------------|---------------------|--|-----|---------|------|-------|
| Parameter | Symbol | Conditions | min | typ | max | Unit |
| | V _{DD} (1) | V _{DD} | 2.0 | | 3.3 | V |
| Supply voltage | V _{DD} (2) | V _{DD} :Serial data retention voltage, see Figure1, *1 | 1.5 | | | V |
| oupply voltage | V _{DD} (3) | V_{DD} :Power-on reset voltage, $t_R \geqq 20 \text{ ms},$ see Figure1, *1 | | | 0.05 | V |
| Input high-level voltage | V _{IH} (1) | CE, CL, DI: V_{DD} = 2.0 V | 1.5 | | 5.5 | V |
| input nigh-level voltage | V _{IH} (2) | CE, CL, DI: V_{DD} = 3.3 V | 1.7 | | 5.5 | V |
| Input low-level voltage | V _{IL} (1) | CE, CL, DI: V_{DD} = 2.0 V | 0 | | 0.4 | V |
| input low-level voltage | V _{IL} (2) | CE,CL,DI:V _{DD} = 3.3 V | 0 | | 0.6 | V |
| Output voltage | V _O (1) | LDA, LDB | 0 | | 5.5 | V |
| Output voltage | V _O (2) | AOA, AOB, OUTA, OUTB | 0 | | 13 | V |
| | f _{IN} (1) | XIN:Sine wave, capacitively coupled | 1.0 | | 13 | MHz |
| Input frequency | f _{IN} (2) | PIA, PIB: Sine wave, capacitively coupled *2 | 1.5 | | 55 | MHz |
| | f _{IN} (3) | PIA, PIB: Sine wave, capacitively coupled *3 | 55 | | 80 | MHz |
| Input amplitude | V _{IN} (1) | XIN: Sine wave, capacitively coupled | 200 | | 600 | mVrms |
| | V _{IN} (2) | PIA, PIB: Sine wave, capacitively coupled *2,3 | 100 | | 600 | mVrms |
| Crystal oscillator frequency | f _{X'tal} | XIN, XOUT: CI \leq 50 Ω CL \leq 16 pF *4 | 4 | 10.24 | 11 | MHz |

Note *1 LC7152NM

| | | FA/FB (serial data inpu | It frequency select bits) | M | Device |
|----|---------------------|-------------------------|---------------------------|-----------------|------------------------------------|
| | | [0] | [1] | V _{DD} | Device |
| *2 | f _{IN} (2) | 1.5 to 23 MHz | 20 to 55 MHz | 2.0 to 3.3 V | LC7152, 7152M, LC7152NM, 7152KM |
| *3 | f _{IN} (3) | | 55 to 80 MHz | 2.7 to 3.3 V | LC7152KM |

*4 Cl is the crystal impedance and CL is the load capacitance.

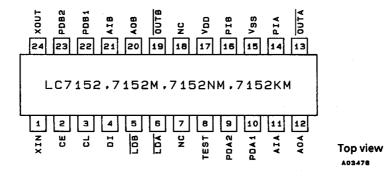
| Parameter | Symbol | Conditions | Rat | ings | | Unit |
|-------------------------------|----------------------|--|-----------------------|------|------|-------|
| i diameter | Symbol | Conditions | min | typ | max | Offic |
| Output high-level voltage | V _{OH} (1) | PDA1, PDB1: I _O = 1 mA | V _{DD} - 1.0 | | | V |
| Suput high-level voltage | V _{OH} (2) | PDA2, PDB2: $I_0 = 2 \text{ mA}$ | V _{DD} - 1.0 | | | V |
| | V _{OL} (1) | PDA1, PDB1: I _O 1 mA | | | 1.0 | V |
| | V _{OL} (2) | PDA2, PDB2: I _O = 2 mA | | | 1.0 | V |
| Output low-level voltage | V _{OL} (3) | OUTA, OUTB: I _O = 1 mA | | | 1.0 | V |
| Output low-level voltage | V _{OL} (4) | $\overline{\text{LDA}}, \overline{\text{LDB}}: I_{O} = 2 \text{ mA}$ | | | 1.0 | V |
| | V _{OL} (5) | AOA, AOB: $I_0 = 0.5$ mA, AIA = AIB = 1.2 V | | | 0.5 | V |
| | V _{OL} (6) | AOA, AOB: $I_0 = 1 \text{ mA}$, AIA = AIB = 1.3 V | | | 0.5 | V |
| | I _{OFF} (1) | $\overline{\text{LDA}}$. $\overline{\text{LDB}}$: V _O = 5.5 V | | | 5.0 | μA |
| Output off-leakage current | I _{OFF} (2) | PDA1, PDB1, PDA2, PDB2: V _O = 0/3.3 V | | 0.01 | 10.0 | nA |
| | I _{OFF} (3) | AOA, AOB, \overline{OUTA} , \overline{OUTB} : V _O = 13 V | | | 5.0 | μA |
| | I _{IH} (1) | CE, CL, DI: V _I = 5.5 V | | | 5.0 | μA |
| | I _{IH} (2) | XIN: V _I = 3.3 V, V _{DD} = 3.3 V | 2.0 | | 6.5 | μA |
| Input high-level current | I _{IH} (3) | PIA, PIB: V _I = 3.3 V, V _{DD} = 3.3 V | 3.5 | | 10.0 | μA |
| | I _{IH} (4) | AIA, AIB: V ₁ = 3.3 V | | 0.01 | 10.0 | nA |
| | I _{IH} (5) | TEST: V _I = 3.3 V, V _{DD} = 3.3 V | | 120 | | μA |
| | I _{IL} (1) | CE, CL, DI: $V_I = 0 V$ | | | 5.0 | μA |
| | I _{IL} (2) | XIN: V _I = 0 V, V _{DD} = 3.3 V | 2.0 | | 6.5 | μA |
| Input low-level current | I _{IL} (3) | PIA, PIB: V _I = 0 V, V _{DD} = 3.3 V | 3.5 | | 10.0 | μA |
| | I _{IL} (4) | AIA, AIB: $V_1 = 0 V$ | | 0.01 | 10.0 | nA |
| | I _{IL} (5) | TEST: V _I = 0 V, V _{DD} = 3.3 V | | | 5.0 | μA |
| Internal feedback resistance | R _f (1) | XIN: $V_{DD} = 3.3 V$ | | 1.0 | | MΩ |
| Internal reedback resistance | R _f (2) | PIA, PIB:V _{DD} = 3.3 V | | 600 | | kΩ |
| Internal pull-down resistance | Rd | TEST: V _{DD} = 3.3 V | | 30 | | kΩ |
| Input capacitance | C _{IN} | XIN, PIA, PIB | | 2.5 | | pF |
| Supply ourroat*1 | I _{DD} (1) | V _{DD} (= 2.0 V):f _{IN} = 55 MHz | | 3.0 | 8.0 | mA |
| Supply current*1 | I _{DD} (2) | V _{DD} (= 3.3 V):f _{IN} = 55 MHz | | 7.0 | 14.0 | mA |
| Current a current #2 | I _{DD} (4) | V _{DD} (= 2.0 V):f _{IN} = 55 MHz | | 1.5 | 4.5 | mA |
| Supply current*2 | I _{DD} (5) | V _{DD} (= 3.3 V):f _{IN} = 55 MHz | | 3.9 | 8.0 | mA |

Electrical Characteristics in the allowable operating ranges

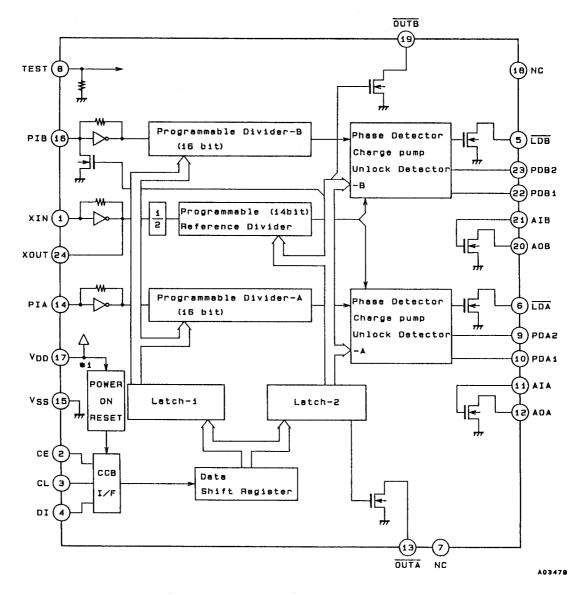
Note *1. Dual PLL operation (both PLL-A and PLL-B), SB= 0, XIN= 10.24 MHz (crystal), PIA and PIB input = 100mVrms at f_{IN}, all other inputs at V_{SS}, all other outputs open.

*2. Standby mode: Single PLL operation (PLL-A operating and PLL-B stopped), SB = 1, XIN = 10.24 MHz (crystal), PIA input = 100mVrms at f_{IN} , all other inputs at V_{SS} , all other outputs open.

Pin Assignment



Equivalent Block Diagram



Pin Functions

| Symbol | Pin No. | | Function | Symbol | Pin No. | Function |
|-----------------|---------|----------------|--------------------|--------|---------|-----------------------------|
| PIB | 16 | Side-B oscill | ator signal input | PDB2 | 23 | Sub charge pump |
| XIN | 1 | Crystal oscill | otor | PDB1 | 22 | Main charge pump |
| XOUT | 24 | | aloi | AIB | 21 | Low-pass filter transistors |
| PIA | 14 | Side-A oscill | ator signal output | AOB | 20 | Low-pass liner transistors |
| V _{DD} | 17 | Power suppl | у | OUTB | 19 | General-purpose output port |
| V _{SS} | 15 | Ground | | LDA | 6 | Side-A unlock detection |
| CE | 2 | Serial data | Chip enable | PDA2 | 9 | Sub charge pump |
| CL | 3 | input | Clock | PDA1 | 10 | Main charge pump |
| DI | 4 | linput | Data | AIA | 11 | Low-pass filter transistors |
| TEST | 8 | IC Test | | AOA | 12 | |
| NC | 7, 18 | No connection | ons | OUTA | 13 | General-purpose output port |
| LDB | 5 | Side-B unloc | k detection | | | |

Pin Description

| Symbol | Pin No. | Function | | Descrip | tion of function | |
|--------------------------|----------------------|--|---|--|---|-----------------------------------|
| PIA | 14 | Side-A local oscillator signal | Side-A programma | 1 | | ranges are as follows. |
| | | input | FA = [0] | FA = [1] | V _{DD} | Device |
| | | | | 20 to 55 MHz | 2.0 to 3.3 V | LC7152, 7152M LC7152NM, 7152KM |
| | | | | 55 to 80 MHz | 2.7 to 3.3 V | LC7152NM, 7152NM |
| | | | FA: Serial data | 55 10 00 10112 | 2.7 10 5.5 V | LOTISZIUM |
| | | | Bits DA0 to DA15 Divider ratio N = | | livider ratios | |
| PIB | 16 | Side-B local-oscillator signal | Side-B programma | | | |
| 110 | | input | The input frequence | | e same as for F | 'IA. |
| | | | $FB(\rightarrow FA)$: Deter | mined by the s | erial data | |
| | | | Bits DB0 to DB15 | | livider ratios | |
| | | | Divider ratio N= | | | |
| | | | Serial data: Bit SB When SB = 1 st | | | ndby mode, side-B is |
| | | | stopped, PIB is p | | | haby mode, side b is |
| | | | When $SB = 0$, no | ormal operation | is selected. | |
| XIN | 1 | Crystal oscillator | Crystal oscillator co | · · · | ' | . , |
| XOUT | 24 | | | | | d above, its compatibility |
| | 10 | Side A main charge nump | With the crys These are PLL characteristics | | ist be thoroughly | |
| PDA1 | 10 | Side-A main charge pump | | | | g the local oscillator signal |
| | | | | | | ency, the charge pump |
| | | | outputs a high-leve | I signal for the | phase error; wh | en lower, the charge pump |
| | | | outputs a low-level | • | | |
| | | Cida D main shares sums | If the two values m | | s go to high-imp | edance. |
| PDB1 | 22 | Side-B main charge pump | • fosc/N > fref or l | eading itive Pulse | | |
| | | | → Fos • fosc/N < fref or l | | | |
| | | | | ative Pulse | | |
| | | | fosc/N = fref and | | | |
| | | | | n-Impedance | | |
| DDAO | | | (*SB = [1] : PDB1 → | | | ' I I I II |
| PDA2 | 9 | Side-A sub charge pump | PLL charge pump unlock condition is | | PLL phase error | signal only when the |
| | | | The unlock detection | | set by serial dat | a bits UL0 and UL1. |
| PDB2 | 23 | Side-B sub charge pump | | | | tion threshold occurs, this |
| | _ | | | | d the phase erro | or signal for the main |
| | | | charge pump is ou | | | |
| | | | The output pulse o charge pump. | f the phase erro | or signal has the | e same polarity as the main |
| LDA | 6 | Side-A unlock detector output | | ck/unlock statu | e | |
| LDA | | | Outputs the PLL lo Locked | | | |
| | | | Unlocked | • | | |
| | | | | | lock/unlock dise | crimination is set by serial |
| | _ | | data bits UL0 and | | | |
| | | | | | to and here it is the | |
| LDB | 5 | Side-B unlock detector output | | | • | data bits UE0 and UE1. |
| LDB | 5 | Side-B unlock detector output | For details, refer to | the description | • | |
| AIA | 5 | Side-A low-pass filter transistor | | the description | n of the serial da | |
| | | | For details, refer to SB = 1: LDB → Op MOS N-channel tra | the description ben ansistor for the | n of the serial da | ta. |
| AIA AOA AIB | 11 12 21 | | • For details, refer to • SB = 1: $\overline{\text{LDB}} \rightarrow \text{Op}$ | the description ben ansistor for the | n of the serial da | ta. |
| AIA AOA AIB OAB | 11 12 21 20 | Side-A low-pass filter transistor Side-B low-pass filter transistor | For details, refer to SB = 1: LDB → Op MOS N-channel tra The AOA and AOB | o the description pen ansistor for the output withstar | n of the serial da PLL filter nd voltage is 13 | ta. V. |
| AIA AOA AIB | 11 12 21 | Side-A low-pass filter transistor Side-B low-pass filter transistor Side-A general purpose | For details, refer to SB = 1: LDB → Op MOS N-channel tra The AOA and AOB These latch the se | o the description pen ansistor for the output withstar rial data bits O/ | n of the serial da PLL filter nd voltage is 13 A and OB that an | ta. |
| AIA AOA AIB OAB | 11 12 21 20 | Side-A low-pass filter transistor Side-B low-pass filter transistor | For details, refer to SB = 1: LDB → Op MOS N-channel tra The AOA and AOB | the description pen ansistor for the output withstar rial data bits O/ d output the dat | n of the serial da PLL filter Ind voltage is 13 A and OB that an a. | ta. V. |

For more information on crystal oscillator : Nihon Dempa Kogyo Co., Ltd.

Continued on next page.

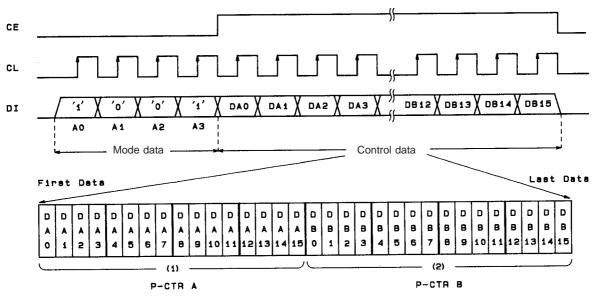
Continued from preceding page.

| Symbol | Pin No. | Function | Description of function |
|------------------------------------|----------|------------------------|--|
| CE *1 | 2 | Chip enable input | • Set this pin high when inputting serial data to the LC7152. |
| CL *1 | 3 | Clock input | Clock for data synchronization when inputting serial data to the LC7152. |
| DI *1 | 4 | Data input | • Input for serial data being sent from the controller to the LC7152. |
| V _{DD} V _{SS} | 17 15 | Power supply Ground | LC7152 power supply pin. |
| TEST | 8 | IC Test input | LC7152 test pin. (Normally V_{SS} or open.) However, divide-by-two XIN frequency is output from the pin OUTA by applying the V_{DD} level voltage after serial data transfer (T0 = T1 = T2 = 0). Crystal oscillation frequency can be checked normally when the pin is left open. |

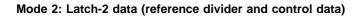
*1 The input "H" voltage and the input "L" voltage on the CE, CL, and DI pins are $V_{IH} = 1.5$ to 5.5V and $V_{IL} = 0$ to 0.4V when $V_{DD} = 2.0$ V. When $V_{DD} = 3.3$ V, then $V_{IH} = 1.7$ to 5.5V and $V_{IL} = 0$ to 0.6V. (Voltage greater than V_{DD} may be applied to V_{IH} .)

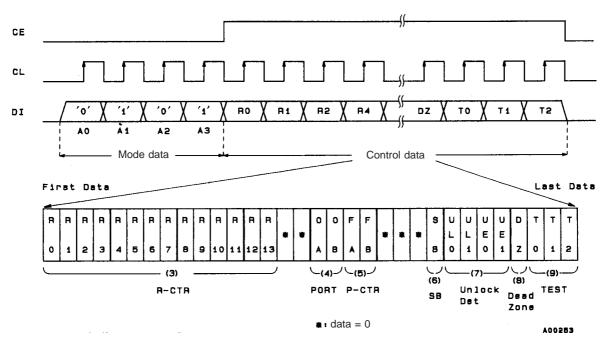
Serial Input Data (PLL Control data) format

Mode1: Latch-1 data (programmable divider data)

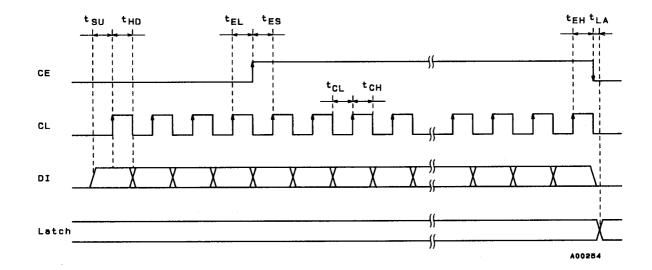


A00252









| Symbol | Parameter | 10.24 MHz crystal | Other crystal frequencies |
|-----------------|------------------------------|-------------------|-------------------------------|
| t _{SU} | Data setup time | At least 0.40 µs | At least 4/f _{X'tal} |
| t _{HD} | Data hold time | At least 0.40 µs | At least 4/f _{X'tal} |
| t _{EL} | Enable low-level pulse width | At least 0.40µs | At least 4/f _{X'tal} |
| t _{ES} | Enable setup time | At least 0.40 µs | At least 4/f _{X'tal} |
| t _{EH} | Enable hold time | At least 0.40 µs | At least 4/f _{X'tal} |
| t _{CL} | Clock low-level pulse width | At least 0.40 µs | At least 4/f _{X'tal} |
| ^t CH | Clock high-level pulse width | At least 0.40 µs | At least 4/f _{X'tal} |
| t _{LA} | Latch propagation delay | Up to 0.40 µs | Up to 4/f _{X'tal} |

Note Perform data transfer after the crystal oscillations normalize. Data transferred before normal oscillations will not be recognized.

Description of Serial Data

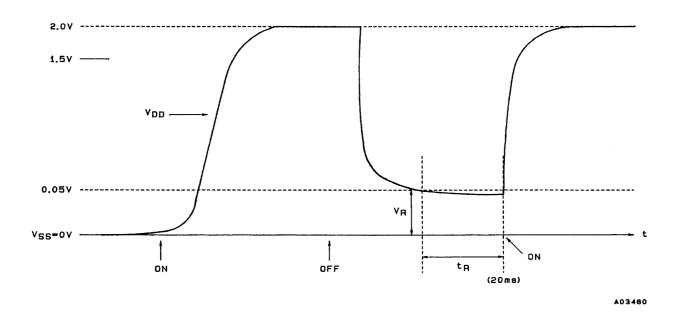
| | Controller/Data | | | | | scription | | | | Related Data |
|-----|--|---|--|--|---|---|--|---|--|-----------------------------|
| (1) | Side-A programmable divider data: DA0 to DA15 | binary The ra | value inge o | ts the side-A in which DA(f divider value CO-A/fref | 0 is the LS | SB. | | | a is a | R0 to R13 |
| (2) | Side-B programmable divider data: DB0 to DB15 | This d binary The ra | ata se value inge o | ts the side-B in which DB(f divider value CO-B/fref | 0 is the LS | SB. | | | a is a | R0 to R13 |
| (3) | Reference frequency data: R0 to R13 | which The ra | R0 is inge o (Actua | ts the referer the LSB. f divider value al divider nun ce frequency | es that ca nber) = (se | n be set i etting) x 2 | is 8 to 16,3 2 | | | UL0 UI1 UE0 UE ⁷ |
| (4) | Output port data: OA, OB | • This d O O • Data 0 | ata de A \rightarrow C B \rightarrow C): oper | termines the OUTA | output on | the gene | eral-purpos | e output p | ort. | |
| (5) | Input frequency range switching data: FA, FB | (FA → | | ritches the inp $FB \rightarrow PIB$) Data [0] [1] Data Data Data Data Data Data Data Data Data Data Data Data Data Data Data Data | Supply v 2.0 1.5 t 20 to | voltage (\ to 3.3 V to 23 MHz o 55 MHz | / _{DD}) z | | | DA0 to DA15 DB0 to DB15 |
| (6) | Standby mode data : SB | • This d • Sl | ata pu B = 1: → S B = 0: | ts the PLL in standby moc ingle PLL op standby moc pual PLL oper | standby r de (LDB pi eration: Si de off | mode. in: open) ide-A ope | rating, side | e-B stoppe | d | |
| | | During | | | | | | | g | |
| (7) | Unlock detection data | This is lock/ui | the p the p hlock c | ower-on rese hase error de discrimination I state is dete | et in the LO etection th . If the thr | C7152NM reshold d | l, SB is "1" lata that is | used for F table is e | PLL exceeded, | |
| (7) | | • This is lock/u the un | the p the p nlock o locked | ower-on rese hase error de discrimination I state is dete Phase error | et in the LO etection th . If the thr | C7152NM reshold d reshold sh | l, SB is "1" lata that is | used for F table is e | ۲L | |
| (7) | data | This is lock/u the un | the p the p nlock c lockec | ower-on rese hase error de discrimination I state is dete Phase error detector threshold | et in the LO etection th . If the thr | C7152NM reshold d reshold sh | l, SB is "1" lata that is nown in the | used for F table is e | PLL exceeded, | |
| (7) | data | This is lock/ui the un UL0 | the p the p nlock c lockec | ower-on rese hase error de discrimination I state is dete Phase error detector threshold 0 | et in the L0 etection th . If the thr ected. 4.0 \leftarrow | C7152NM reshold d reshold sh XIN : f) 7.2 ← | I, SB is "1" lata that is nown in the KIN [MHz] 8.0 ← | used for F table is e example 10.24 | PLL exceeded, unit : µs 12.8 ← | |
| (7) | data | This is lock/ui the un UL0 0 1 | UL1 0 0 | ower-on rese hase error de discrimination I state is dete Phase error detector threshold 0 ±4/f _{X'tal} | t in the L0 etection th b. If the thr ected. 4.0 \leftarrow ± 1.00 | C7152NM reshold d reshold sh XIN : f) 7.2 ← ±0.55 | I, SB is "1" lata that is nown in the KIN [MHz] 6 8.0 ← ±0.50 | used for F table is e example 10.24 \leftarrow ± 0.39 | PLL exceeded, unit : μ s 12.8 \leftarrow \pm 0.31 | |
| (7) | data | This is lock/ui the un UL0 | the p the p nlock c lockec | ower-on rese hase error de discrimination I state is dete Phase error detector threshold 0 | et in the L0 etection th . If the thr ected. 4.0 \leftarrow | C7152NM reshold d reshold sh XIN : f) 7.2 ← | I, SB is "1" lata that is nown in the KIN [MHz] 8.0 ← | used for F table is e example 10.24 | PLL exceeded, unit : µs 12.8 ← | |
| (7) | data | This is lock/ui the un UL0 0 1 0 1 | UL1 0 1 Note | ower-on reset hase error de discrimination I state is dete Phase error detector threshold 0 ±4/f _{X'tal} ±16/f _{X'tal} | t in the L0 etection th . If the three ected. 4.0 \leftarrow ± 1.00 ± 4.00 ± 16.00 | C7152NM reshold d reshold st XIN : f) 7.2 ← ±0.55 ±2.22 ±8.88 | I, SB is "1" ata that is hown in the KIN [MHz] 0 8.0 ← ±0.50 ±2.00 ±8.00 | used for F a table is a example 10.24 \leftarrow ± 0.39 ± 1.56 ± 6.25 | PLL exceeded, unit : µs 12.8 ← ±0.31 ±1.20 ±5.00 | |
| (7) | data | This is lock/u the un UL0 0 1 0 1 (Note) The do of time length | UL1 0 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 0 0 0 1 0 | ower-on reset hase error de discrimination I state is dete Phase error detector threshold 0 $\pm 4/f_{X'tal}$ $\pm 16/f_{X'tal}$ that if the da | tin the L0 etection the . If the three ected. 4.0 \leftarrow ± 1.00 ± 16.00 ta change (\emptyset E) sign LDA and However, v | C7152NM reshold d reshold st XIN : f) 7.2 ← ±0.55 ±2.22 ±8.88 s in lock hal can be LDB pins when ULC | I, SB is "1" lata that is hown in the N [MHz] 4.00 ± 0.50 ± 2.00 ± 8.00 state, the F extended State, the F | used for F a table is a example 10.24 \leftarrow ± 0.39 ± 1.56 ± 6.25 PLL will be by a certa a determin | PLL exceeded, unit : μ s 12.8 \leftarrow ± 0.31 ± 1.20 ± 5.00 e unlocked ain amount es the se error is | t |
| (7) | data : UL0, UL1 | This is lock/u the un UL0 0 1 0 1 (Note) The do of time length | UL1 0 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 0 0 0 1 0 | ower-on rese hase error de discrimination I state is dete Phase error detector threshold 0 ±4/f _{X'tal} ±64/f _{X'tal} that if the da orarily. d phase error putput on the s extension. H d, and is outp | t in the L0 tetection th If the thr teted. 4.0 ← ±1.00 ±4.00 ±16.00 ta change (ØE) sign LDA and However, vout directly ce Cy | C7152NM reshold d reshold sh XIN : f) 7.2 ← ±0.55 ±2.22 ±8.88 rs in lock hal can be LDB pins when ULC , Refere fref [| I, SB is "1" lata that is lata that is hown in the (IN [MHz]] 8.0 ± 0.50 ± 2.00 ± 8.00 state, the F e extended S. This data $= UL1 = 0$ Ince freque kHz] exam | used for F e table is e example 10.24 \leftarrow ± 0.39 ± 1.56 ± 6.25 PLL will be by a certa a determin 0, the pha unit : m ency : ple | PLL exceeded, unit : μ s 12.8 \leftarrow ± 0.31 ± 1.20 ± 5.00 e unlocked ain amount es the se error is s | t |
| (7) | data : UL0, UL1 | This is lock/u the un UL0 0 1 0 1 (Note) • The de of time length not ex | UL1 0 0 0 1 1 UE1 | ower-on rese hase error de discrimination I state is dete Phase error detector threshold 0 ±4/f _{X'tal} ±16/f _{X'tal} ±64/f _{X'tal} that if the da orarily. d phase error output on the s extension. H d, and is outp | tin the L0 tetection the L1 fithe three teted. 4.0 \leftarrow ± 1.00 ± 4.00 ± 16.00 ta change (@E) sign LDA and However, would directly ce Cy 1 | C7152NM ireshold d reshold sh XIN : f) 7.2 ← ±0.55 ±2.22 ±8.88 is in lock in lock in lock in lock Reference fref [kHz | I, SB is "1" lata that is nown in the (IN [MHz]] 8.0 ± 0.50 ± 2.00 ± 2.00 ± 8.00 state, the F e extended s. This data D = UL1 = 0 Ince freque kHz] exam 5 kHz | used for F e table is e example 10.24 \leftarrow ± 0.39 ± 1.56 ± 6.25 PLL will be by a certa a determin 0, the pha unit : m ency : ple 12.5 kHz | PLL exceeded, unit : μ s 12.8 \leftarrow ± 0.31 ± 1.20 ± 5.00 e unlocked ain amount es the se error is s | t |
| (7) | data : UL0, UL1 | This is lock/u the un UL0 0 1 0 1 (Note) • The de of time length not ex UE0 0 | UL1 0 0 1 1 0 0 0 1 1 0 0 0 0 1 1 0 0 0 0 | ower-on reset hase error de discrimination I state is dete Phase error detector threshold 0 $\pm 4/f_{X'tal}$ $\pm 16/f_{X'tal}$ $\pm 64/f_{X'tal}$ that if the datorarily. d phase error output on the s extension. If d, and is output Reference frequence fref 4 × (1/fref | tin the L0 tetection the L1 the three teted. 4.0 \leftarrow ± 1.00 ± 4.00 ± 16.00 ta change (@E) sign LDA and However, would directly ce Cy 1 eff) | C7152NM ireshold d reshold sh XIN : f) 7.2 ← ±0.55 ±2.22 ±8.88 is in lock hal can be LDB pins when ULC r. Refere fref [kHz 4.0* | I, SB is "1" lata that is nown in the KIN [MHz] 8.0 \leftarrow ± 0.50 ± 2.00 ± 8.00 state, the F e extended S. This data $=$ UL1 = (ence freque kHz] exam 5 kHz 0.8 | used for F e table is e example 10.24 \leftarrow ± 0.39 ± 1.56 ± 6.25 PLL will be by a certa a determin 0, the pha unit : m ency : ple 12.5 kHz 0.32 | PLL exceeded, unit : μ s 12.8 \leftarrow ± 0.31 ± 1.20 ± 5.00 e unlocked ain amount es the se error is s | t |
| (7) | data : UL0, UL1 | This is lock/u the un UL0 0 1 0 1 (Note) The da of time length not ex UE0 0 1 | UL1 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 1 1 0 | ower-on reset hase error de discrimination I state is dete Phase error detector threshold 0 $\pm 4/f_{X'tal}$ $\pm 16/f_{X'tal}$ $\pm 64/f_{X'tal}$ that if the datorarily. d phase error output on the s extension. H d, and is output Reference frequence fref 4 × (1/fref 8 × (1/fref | tin the L0 tetection the L1 the three teted. 4.0 \leftarrow ± 1.00 ± 4.00 ± 16.00 ta change (@E) sign LDA and However, wo but directly ce (y) | C7152NM reshold d reshold sh XIN : f) 7.2 ← ±0.55 ±2.22 ±8.88 s in lock hal can be LDB pins when ULC r Refere fref [kHz 4.0* 8.0 | I, SB is "1" lata that is nown in the KIN [MHz] 8.0 \leftarrow ± 0.50 ± 2.00 ± 8.00 state, the F e extended S. This data $0 = UL1 = 0$ ence freque kHz] exam 5 kHz 0.8 1.6 | used for F e table is e example 10.24 \leftarrow ± 0.39 ± 1.56 ± 6.25 PLL will be by a certa a determin 0, the pha unit : m ency : ple 12.5 kHz 0.32 0.64 | PLL exceeded, unit : μ s 12.8 \leftarrow ± 0.31 ± 1.20 ± 5.00 e unlocked ain amount es the se error is s | t |
| (7) | data : UL0, UL1 | This is lock/u the un UL0 0 1 0 1 (Note) • The de of time length not ex UE0 0 | UL1 0 0 1 1 0 0 0 1 1 0 0 0 0 1 1 0 0 0 0 | ower-on reset hase error de discrimination I state is dete Phase error detector threshold 0 $\pm 4/f_{X'tal}$ $\pm 16/f_{X'tal}$ $\pm 64/f_{X'tal}$ that if the datorarily. d phase error output on the s extension. If d, and is output Reference frequence fref 4 × (1/fref | tin the L0 tetection the L1 fithe three 4.0 \leftarrow ± 1.00 ± 4.00 ± 16.00 ta change (@E) sign LDA and However, would directly ce cy 1 eff eff afff | C7152NM ireshold d reshold sh XIN : f) 7.2 ← ±0.55 ±2.22 ±8.88 is in lock hal can be LDB pins when ULC r. Refere fref [kHz 4.0* | I, SB is "1" lata that is nown in the KIN [MHz] 8.0 \leftarrow ± 0.50 ± 2.00 ± 8.00 state, the F e extended S. This data $=$ UL1 = (ence freque kHz] exam 5 kHz 0.8 | used for F e table is e example 10.24 \leftarrow ± 0.39 ± 1.56 ± 6.25 PLL will be by a certa a determin 0, the pha unit : m ency : ple 12.5 kHz 0.32 | PLL exceeded, unit : μ s 12.8 \leftarrow ± 0.31 ± 1.20 ± 5.00 e unlocked ain amount es the se error is s | t |

Continued on next page.

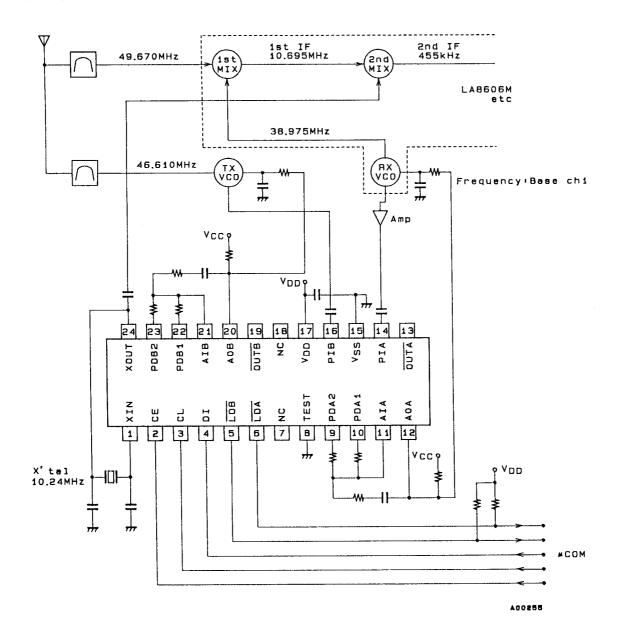
| No. | Controller/Data | | | Description | Related Data |
|-----|-------------------------------|--|-----------------------------------|---|--------------|
| (8) | Dead zone control data: DZ | This data controls t (DZA < DZB) DZ 0 1 | he phase co Mode DZA DZB | omparator dead zone. | |
| (9) | IC test data: T0, T1, T2 | concerned about th Assume that Te | is data. 0 = T1 = T2 | ing data. The user does not need to be 2 = 0. e either at V _{SS} or left open. | |

Continued from preceding page.

Power-on Reset supply voltage



- Power-on reset is performed when the supply voltage V_{DD} exceeds 2.0 V by power application after the V_{DD} has once fallen under 0.05 V and kept the level for at least 20ms. • Latch data is retained when the V_{DD} is 1.5 V, where power-on reset is not performed.



Sample Application Circuit (FCC: 10 ch 46/49 MHz cordless telephone)

Example: FCC 1-channel 46/49 MHz cordless telephone base station (See diagram in the preceding page.) for fref: 5 kHz, RX VCO: 38.975 MHz, TX VCO: 46.610 MHz

Programmable Divider Data

(1) NA = $\frac{\text{fVCO} - \text{A}}{\text{fref}} = \frac{\text{RX VCO}}{\text{fref}} = \frac{38.975\text{MHz}}{5\text{kHz}} = 7795 \text{ (DA0 to DA15)}$ (1E73)Hex

- (2) NB = $\frac{\text{fVCO} \text{B}}{\text{fref}} = \frac{\text{TX VCO}}{\text{fref}} = \frac{46.610\text{MHz}}{5\text{kHz}} = 9322 \text{ (DB0 to DB15)}$ (246A)Hex
- (3) Reference frequency data

$$NR = \left(\frac{fX' tal}{fref}\right) \div 2 = \frac{10.24MHz}{5kHz} \div 2 = 1024 (R0 to R13)$$
(400)Hex

- (4) Output port data General-purpose output port: Open (OA = 0, OB = 0)
- (5) Input frequency range select bits FA = FB = 1
- (6) Standby mode
- During standby (SB = 1)(7) Unlock detector output

Extends the phase error signal by 6.4ms if a phase error of $\pm 6.25 \ \mu s$ or more is generated. : UI (

$$UL0 = UL1 = 1$$

- : UE0 = 0, UE1 = 1(8) Dead-zone control data
 - DZA mode : DZ = 0
- (9) LSI test data: T0 = T1 = T2 = 0

(1) Mode 1: Latch-1 data

| D | D | 5 | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | 10 | D | D | D | D | D | D | D | D |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|---|---|---|---|---|---|---|----|---|---|----|----|----|----|----|----|
| A | A | V | A | A | A | A | A | A | A | A | A | A | A | A | A | B | 8 | B | 8 | B | 8 | 8 | 18 | 8 | 8 | B | B | 8 | 8 | 8 | 8 |
| 0 | 1 | D | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | O | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | i | 0 | 0 |

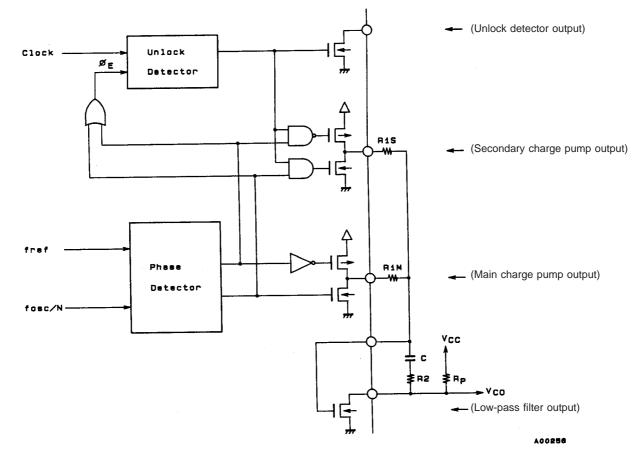
(2) Mode 2: Latch-2 data

| P | A | R | R | R | A | A | A | A | R | A | R | A | R | | | 0 | 0 | F | F | | | | s | υ | υ | U | U | ۵ | т | т | т |
|------|---|---|---|---|---|---|---|---|---|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------|
| | | | _ | | | | | | | | | | | | • | | | | | | ۰ | | | L | L | E | Е | | | | т 2 |
| | 1 | 5 | Э | 4 | 5 | 6 | 1 | 8 | 9 | 10 | 11 | 12 | 13 | | | | 8 | A | в | | | | в | 0 | 1 | 0 | 1 | Z | 0 | 1 | 2 |
| ¦o | 0 | 0 | 0 | 0 | 0 | o | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | o | 0 |
| | | | 1 | 1 | | | l | l | | | l | 1 | | | l | i | | | ļ | | | | 1 | | | | | 1 | | | 1 |

: data = 0

A00256

Dual Charge Pump Descriptions



If an unlock state is detected at channel switch, the sub-charge pump operates, R1M/R1S becomes R1, low-pass filter's time constant is reduced, and the lockup accelerates.

When the circuit is locked, side-band characteristics and modulation characteristics are improved by making the sub-charge pump off, i.e., floating, R1M to be R1, and increasing low-pass filter's time constant.

Device Comparison

| Device | Operating frequency | | | D | |
|----------|---------------------|--------------|---|----------------|---------|
| | FA/FB = 0 | FA/FB = 1 | | Power-on reset | Package |
| | 1.5 to 23 MHz | 20 to 55 MHz | 55 to 80 MHz | onoun | |
| LC7152 | Yes | Yes | No | No | DIP24S |
| LC7152M | Yes | Yes | No | No | MFP24S |
| LC7152NM | Yes | Yes | No | Yes | MFP24S |
| LC7152KM | Yes | Yes | Yes (V _{DD} = 2.7 to 3.3 V) | No | MFP24S |

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of June, 1999. Specifications and information herein are subject to change without notice.